REMARKS

Claims 1-8 and 10-24 are pending in the application. Claims 1-6 are withdrawn from consideration as being directed to non-elected inventions. In the Office Action of November 8, 2002, the Examiner made the following disposition:

A.) Rejected claims 7, 8, 10, 11, 16, and 19-24 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* in view of *Hotchkiss*.

B.) Rejected claims 12, 13, and 17 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* and *Hotchkiss*, and further in view of *Nishikawa et al.* and *Denning et al.*

C.) Rejected claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* and *Hotchkiss*, and further in view of *Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura*.

D.) Rejected claim 18 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* and *Hotchkiss*, and further in view of *Jackson*.

Applicant respectfully traverses the rejections. Applicant addresses the Examiner's disposition as follows:

A.) Rejection of claims 7, 8, 10, 11, 16, and 19-24 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* in view of *Hotchkiss*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7, as amended, claims a method of producing a semiconductor apparatus comprising forming metal ball bumps in direct contact with a circuit pattern of a semiconductor device formed on a semiconductor substrate in a semiconductor wafer state. A resin film is formed on a circuit pattern forming surface of the semiconductor device so as to seal spaces between the metal ball bumps and to become thinner than a height of the metal ball bumps. The surfaces of the metal ball bumps projecting out from the resin film are cleaned. After the cleaning step, solder layers different in composition from the metal ball bumps are formed on the surfaces of the metal ball bumps. After the solder layers forming step, the semiconductor substrate is cut into unit semiconductor chips, each semiconductor chip having at least one of the semiconductor device. After the cutting step, at least one of the semiconductor chips is mounted on a mounting board from a bump forming surface side of the semiconductor chip so as to connect the semiconductor chip to the mounting board at the bumps without the use of a resin formed between and contacting both the semiconductor chip and the mounting board.

As illustratively depicted in Applicant's Fig. 1, Applicant's semiconductor chip 100 is mounted to the mounting board 200 via bumps 116b and solder layers 119, without the use of a resin formed to both the semiconductor chip 100 and the mounting board 200. Accordingly, as depicted, there is a space between the semiconductor chip 100 and the mounting board 200 surrounding the bumps 116. As described in Applicant's specification, since Applicant claims mounting via bumps and solder layers without using a sealing resin, Applicant's claim 7 reliably relieves thermal stress between a semiconductor device and a mounting base without the use of a sealing resin, reduces the connection resistance, and increases the strength of the joint portion. (Page 47, line 21 - page 48, line 1).

Further, since the method of claim 7 reinforces the bases of the bumps with resin, it is possible to suppress the rise of electrical resistance and the decline of joint strength at the bump joint interfaces and to improve connection reliability. (Page 48, lines 2-7).

This is clearly unlike *Hayes* in view of *Hotchkiss*, which fails to disclose Applicant's claimed steps. Referring to *Hayes* Figs 2 and 3, *Hayes* discloses forming solder columns 3, instead of bumps, to connect to a circuit pattern 2 of a semiconductor device 5. A polymer film 4 is then deposited between the solder columns 3. A top surface of the polymer film 4 is then removed to expose tops of the solder columns 3. Then, solder ball bumps 9 are formed onto the tops of the solder columns 3.

Thus, unlike Applicant's claim 7, *Hayes's* solder ball bumps 9 are neither formed in direct contact with *Hayes's* circuit pattern 2 (unlike Applicant's claimed step 1), nor sealed by resin film 4 (unlike Applicant's claimed step 2), nor cleaned (unlike Applicant's claimed step 3). Instead *Hayes's* solder ball bumps 9 are formed on top of solder columns 3 that are formed in direct contact with *Hayes's* circuit pattern 2.

The Examiner argues that *Hotchkiss et al.* teaches that solder balls and solder columns are funtional equivalents, however, Applicant respectfully disagrees. As illustratively depicted in Applicant's Figure 1, when Applicant's solder layer 119 melts to seal the solder ball 116b to the mounting board 200, a large surface area of the solder ball 116b is sealed to the solder layer 119. This surface area is greater than if the solder ball had the shape of a solder column. Therefore, the claimed combination of solder ball 116b with a solder layer 119 formed thereon provides a beneficial improvement over *Hayes's* solder column. Applicant respectfully submits that a solder column is not functionally equivalent to a solder ball for purposes of interpreting claim 7.

Therefore, for at least this reason, *Hayes* in view of *Hotchkiss* fails to disclose or suggest claim 7.

Further, nowhere does *Hayes* in view of *Hotchkiss* disclose or suggest mounting a semiconductor device to a mounting board as claimed in claim 7. Nowhere does *Hayes* disclose mounting its semiconductor package to a mounting board. Although *Hotchkiss* discloses mounting a substrate 111 to a ball grid array package 112, *Hotchkiss* still fails to disclose or suggest the steps of claim 7. Therefore, *Hayes* in view of *Hotchkiss* also fails to disclose or suggest claim 7 for this reason.

Claims 8, 10-11, 16, and 19-21 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Claims 22-24 have been cancelled.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

B.) Rejection of claims 12, 13, and 17 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* and *Hotchkiss*, and further in view of *Nishikawa et al.* and *Denning et al.*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is allowable over *Hayes* in view of *Hotchkiss* as discussed above.

Nishikawa et al. and *Denning et al.*, taken singly or in combination, still fail to disclose or suggest Applicant's claimed solder ball bumps and solder layer that are formed to connect to the circuit pattern, or mounting of a semiconductor chip to a mounting board as claimed. Thus, *Hayes* in view of *Hotchkiss*, and further in view of *Nishikawa et al.* and *Denning et al.* still fails to disclose or suggest Applicant's independent claim 7.

Claims 12, 13, and 17 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

C.) Rejection of claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* and *Hotchkiss*, and further in view of *Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is allowable over *Hayes* in view of *Hotchkiss*, and further in view of *Nishikawa et al.* and *Denning et al.* as discussed above.

Okumura still fail to disclose or suggest Applicant's claimed solder ball bumps and solder layer that are formed to connect to the circuit pattern, or mounting of a semiconductor chip to a mounting board as claimed. Thus, *Hayes* in view of *Hotchkiss*, and further in view of *Nishikawa et al.* and *Denning et al.*, and further in view of *Okumuira* still fails to disclose or suggest Applicant's independent claim 7.

Claims 14 and 15 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

D.) Rejection of claim 18 under 35 U.S.C. §103(a) as being unpatentable over *Hayes* and *Hotchkiss*, and further in view of *Jackson*:

Applicant respectfully disagrees with the rejection.

Applicant's independent claim 7 is allowable over *Hayes* in view of *Hotchkiss* as discussed above.

Jackson still fail to disclose or suggest Applicant's claimed solder ball bumps and solder layer that are formed to connect to the circuit pattern, or mounting of a semiconductor chip to a mounting board as claimed. Thus, *Hayes* in view of *Hotchkiss*, and further in view of *Jackson* still fails to disclose or suggest Applicant's independent claim 7.

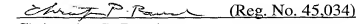
Claim 18 depends directly or indirectly from claim 7 and is therefore allowable for at least the same reasons that claim 7 is allowable.

Applicant respectfully submits that the rejection has been overcome and requests that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 7-8 and 10-21 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Asst. Commissioner for Patents, Washington, D.C. 20231 on February 7, 2003.

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